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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/603,579
Filing Date: June 25, 2003
Appellant(s): BADETS ET AL.

William A. Munck (Reg. No. 39,308)
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 1/15/2009 appealing from the Office action mailed 8/5/2008.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-2, 24-29 and 33-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Dai et al. (USP 6,469,585). Figure 3 of Dai et al. reference shows a phase shifter circuit comprising an input for receiving an input signal (Vin input signal) having a specified oscillation frequency (see figures 4 and 5), an output delivering an output signal (Vout) having said specified oscillation frequency (see figures 4 and 5) and having a variable phase shift with respect to said input signal (figures 4 and 5 shows a delay relationship between the input and output signals), at least one control input receiving a control signal (Vcntrl) which controls the phase shift of said output signal with respect to said input signal, and a synchronized oscillator (M1, M7 and cross coupled transistors M5 and M6, i.e., astable multivibrator, maintains the oscillation of the output signal, thus, the limitation of synchronized oscillator is met) having at least a synchronization input coupled said input of said variable phase shifting circuit, at least one output coupled to said output of said output of the variable phase shifting circuit, said synchronized oscillator having a variable free running oscillation frequency controlled by said

control signal (the oscillation frequency of the oscillator is being control by the control signal) as called for in claims 1 and 24-25.

2. Regarding claims 2 and 26-29, the first and second branches are seen as M2-M3; M8-M9 and means for delivering into the first and second branch a respective quiescent current of a same specified value are transistors M1, M4; and M7 and 10 controlled by the control signal.

3. Regarding claim 33, the synchronized oscillator comprises the astable multivibrator having a first branch (anticipated by M2, M3 of Dai et al.) and a second branch (anticipated by transistors M8, M9 of Dai et al.) connected in parallel in between the power supply (Vdd) and ground.

4. Regarding claims 34-36, the first and second branches are seen as M2-M3; M8-M9 and means for delivering into the first and second branch a respective quiescent current of a same specified value are transistors M1, M4; and M7 and 10 controlled by the control signal.

***Response to Arguments***

**5. Claims 1-2, 24-29 and 33-36 are rejected under 35USC 102(e) as being anticipated by Dai et al. (USP 6,469,585).**

6. Appellant argues that Dai et al. reference is not a variable phase shifter is not persuasive. Figure 3 of Dai et al. is a variable delay circuit with delay time is variably controlled by the control signal (VCNTRL, see column 4, lines 23-27). This is evidently shown in figures 4 and 5 in which the input and output signals are at a relatively phase shifted with one another. Therefore, the limitation of a variable phase shifter circuit is fully met.

7. Appellant argues that because the strength of the memory element 35 remains relatively constant (Dai et al., column 5, line 67 to column 6, line 6) , hence, the memory element 35 is not

a synchronized oscillator that has a variable free running oscillation frequency that is controlled by a control signal is not persuasive. The fact that the cross coupled transistors M5 and M6 has a relatively constant strength is to delay the switching states between the input and output signals from t1 to t2 as shown in figures 4 and 5. The cross coupled transistors M5 and M6 provides a feedback connection in which the output signal is fed back to the input termial so that the signal is oscillating within the loop, thus, constituting a synchronized oscillator. The control signal (VCNTRL) in combination with the input signal changes the switching state inside the loop, hence, control the free running oscillation frequency (figures 4 and 5 show the frequency of input and output signals are maintained at a constant rate). Note, Appellant's own disclosure in figure 5 shows a cross coupled transistors Q2 and Q4 providing a feedback connection in which the output signal is fed back to the input terminal to achieve synchronized oscillation. Therefore, the limitation of synchronized oscillator is also met.

8. For these reasons, Dai et al. reference fully anticipates the claimed limitations. Therefore, the rejection of claims 1-2, 24-29 and 33-36 are deemed proper.

9. Claims 3, 30-32 and 37-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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